REMARKS

In an Office Action mailed on August 28, 2002, claim 19 was rejected under 35 U.S.C. § 112, second paragraph; claims 7-9, 13-15, 18 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tamura in view of Dara; and claims 20-27 were allowed. Claim 19 has been amended to overcome the § 112 rejection. The § 103 rejections are discussed below.

In response to the last Reply, the Examiner states that in regards to Tamura, "specifically, there is no teaching how the output of the phase comparator is to control the variable delay circuits." Office Action, 2. However, Applicant disagrees with this statement, as it is clear from Figures 11 and 14, cited by the Examiner, that the phase comparator 503 controls switches in the variable delay circuits 5302 and 5303 (*see* Figure 14 of Tamura) to control the delay of these circuits. Tamura states, "the variable delay circuits 5302 and 5303 are identical in configuration, and provide the same amount of delay in accordance with an output from the phase comparator circuit 5301." Tamura, 19:17-20. Thus, it is clear that Tamura teaches adjusting a delay by using a phase comparator 5301 to control switches to select the appropriate number of inverters in the delay circuits 5302 and 5303.

To the contrary, Dara teaches a phase converter 61 that produces a signal that has a duty cycle that is proportional to the phase difference between two signals. Dara, 12:21-27. This control signal from the phase comparator 61, in turn, causes an output signal of filter circuit 62 to provide "a control voltage, having a voltage level proportional to the phase difference between the signals carried by signal lines 57 and 71, to adjust the *frequency* at which VCO64 oscillates." (emphasis added). *Id.*, 34-39. Dara further states, "more accurately, filter circuit 62 provides the necessary control voltage to the VCO64 to bring the output signal of VCO64 to the desired frequency." Thus, Dara describes a scheme for adjusting a *frequency* for purposes of synchronizing the phases of two signals. In contrast, Tamura teaches adjusting a delay to adjust timing between two signals. Therefore, not only does Tamura clearly teach a way to adjust phase from the output of a comparator, the delay adjustment technique described in Tamura is quite different from the delay adjustment technique: adjusting a delay rather than adjusting a

frequency. It is noted that if the frequency adjustment of Dara was incorporated into the circuitry of Tamura, the principle of operation of the circuitry of Tamura would be changed. In this manner, the circuitry in Tamura does not change a frequency of a data or clock signal. Thus, changing the frequency of the data or clock signal of Tamura would change the principle of operation of the prior art invention being modified, thereby making the proposed modification improper. *In re Ratti*, 123 USPQ 349 (CCPA 1959); M.P.E.P. § 2143.01.

Therefore, for at least these reasons, withdrawal of the § 103(a) rejections is requested.

CONCLUSION

In view of the foregoing, withdrawal of the §§ 112 and 103 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0294US).

Respectfully submitted,

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CLAIM AMENDMENTS

Claim 19 has been amended as follows:

19. (Amended Twice) The method of claim 13, further comprising:

causing the data bit signal to indicate a predetermined data pattern concurrently with the using the data bit signal and the first strobe signal to generate said at least one pulse train signal.